WE CLAIM:

1. A semiconductor integrated circuit comprising:
   contact pads located over active components; and
   the position of said pads selected to provide control and distribution of power to said active components below said pads.

2. The semiconductor integrated circuit according to Claim 1, wherein said contact pad positions further provide dissipation of thermal energy released by said active components.

3. A semiconductor integrated circuit comprising:
   contact pads located over active components; and
   said pads positioned to minimize the distance for power delivery between a selected pad and one or more corresponding active components, to which said power is to be delivered.

4. The semiconductor integrated circuit according to Claim 3, wherein said minimum distance further maximizes dissipation of thermal energy released by said active components.

5. A semiconductor integrated circuit comprising:
   a laterally organized power transistor;
   an array of power supply contact pads distributed over said power transistor;
   means for providing a distributed, predominantly vertical current flow from said contact pads to said transistor; and
   means for connecting a power source to each of said contact pads.

6. A semiconductor device comprising:
   a semiconductor substrate;

an active circuit fabricated on said substrate and comprised of an integrated power transistor, said circuit having at least one metallization layer forming a plurality of first and second electrodes of said transistor;

a first bus connecting all of said first electrodes, and a second bus connecting all of said second electrodes, each bus connected to said respective electrode by metal-filled vias, whereby said buses are positioned directly over said transistor;

a mechanically strong, electrically insulating film overlaying said circuit, said transistor, and said buses;

a plurality of contact pads distributed over each of said buses, each of said pads having a stack of stress-absorbing metal layers, the outermost layer being metallurgically attachable, and a connection to the underlying bus through openings in said insulating film, said openings positioned substantially vertically over at least one of said vias; and

at least one connecting member attached to said contact pads, whereby the electrical current path and resistance from said member to said electrodes are minimized, improving the electrical characteristics of said power transistor.

7. The device according to Claim 6 wherein said substrate is selected from a group consisting of silicon, silicon germanium, gallium arsenide, and any other semiconductor material customarily used in electronic

device production.

8. The device according to Claim 6 wherein said circuit comprises a plurality of active and passive electronic components arranged horizontally and vertically.

9. The device according to Claim 6 wherein said power transistor is laid out horizontally, having said electrodes arranged in a plurality of metal bands substantially parallel to each other.

10. The device according to Claim 9 wherein said power transistor comprises electrical current flowing horizontally through said electrodes and said semiconductor between said electrodes.

11. The device according to Claim 6 wherein said at least one metallization layer is made of pure or alloyed copper, aluminum, nickel, or refractory metals.

12. The device according to Claim 6 wherein said electrically insulating film further serves as the protective overcoat of said integrated circuit.

13. The device according to Claim 6 wherein said electrically insulating film comprises materials selected from a group consisting of silicon nitride, silicon oxynitride, silicon carbon alloys, polyimide and sandwiched films thereof.

14. The device according to Claim 13 wherein said electrically insulating film is between about 400 and 1500 nm thick.

15. The device according to Claim 6 wherein said stack of metal layers of said contact pads comprise a layer of seed metal on said bus bar, promoting adhesion to said bus bars and inhibiting migration of overlying metals to said bus bar, at least one stress-absorbing metal layer, and an outermost metallurgically attachable

metal layer.

16. The device according to Claim 15 wherein said seed metal layer is selected from a group consisting of tungsten, titanium, titanium nitride, molybdenum, chromium, and alloys thereof.

17. The device according to Claim 16 wherein said layer of seed metal is between about 200 and 500 nm thick.

18. The device according to Claim 15 wherein said stress-absorbing metal layer comprises at least one layer selected from a group consisting of copper, nickel, aluminum, and alloys thereof.

19. The device according to Claim 18 wherein said stress-absorbing metal layer is between about 2 and 35 μm thick.

20. The device according to Claim 15 wherein said outermost metal layer is metallurgically bondable or solderable.

21. The device according to Claim 20 wherein said outermost bondable metal layer is selected from a group consisting of pure or alloyed aluminum, gold, palladium, and silver.

22. The device according to Claim 20 wherein said solderable metal layer is selected from a group consisting of palladium, gold, silver and platinum.

23. The device according to Claim 20 wherein said outermost layer is between about 500 and 2800 nm thick.

24. The device according to Claim 6 wherein said connecting member is a bonding wire or a solder ball.

25. The device according to Claim 24 wherein said bonding wire is selected from a group consisting of pure or alloyed gold, copper, and aluminum.

26. The device according to Claim 24 wherein said solder ball is selected from a group consisting of tin, tin

alloys including tin/copper, tin/indium, tin/silver, tin/bismuth, tin/lead, and conductive adhesive compounds.

27. A method for fabricating an active circuit on a semiconductor substrate, said circuit having an integrated power transistor and at least one metallization layer forming a plurality of first and second electrodes of said transistor, comprising the steps of:

forming a first bus connecting all of said first electrodes and a second bus connecting all of said second electrodes, each bus connected to said respective electrode by metal-filled vias, thereby positioning said buses directly over said transistor;

depositing a mechanically strong, electrically insulating film overcoating said circuit, said transistor and said buses;

forming a plurality of openings through said film to said buses, each of said openings positioned substantially vertically over at least one of said vias;

filling said openings by depositing a stack of stress-absorbing metal layers on said film, the outermost layer being metallurgically attachable;

forming a plurality of contact pads from said stack of layers, each pad comprising at least one of said openings;

attaching at least one connecting member to said contact pads, thereby creating an electrical current path from said member to said electrodes of minimum length and minimum resistance, thus

improving the electrical characteristics of said power transistor.

28. The method according to Claim 27 wherein said depositing of said stack of metal layers comprises the steps of:

depositing a seed metal layer on the surface of said substrate;

forming a plating pattern over said seed metal layer, said plating pattern resulting in exposed portions of said seed metal layer and blocking the rest of said seed metal layer;

covering said exposed portions of said seed metal layer with an electrically conductive, stress-absorbing support layer;

covering said support layer with a metallurgically attachable layer; and

removing said blocked portions of said seed metal layer.

29. The method according to Claim 27 wherein said attaching of a connecting member comprises the step of either bonding a wire to said contact pad, or reflowing a solder ball to said pad.